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ABSTRACT OF THE DISCLOSURE

A method of manufacturing a semiconductor device having a first and second transistor of an ESD protection and internal circuit respectively. The method includes the steps of providing a substrate, forming gates of the first and second transistor on the substrate, depositing a mask layer and patterning the mask layer using one single mask to remove the mask layer on the gates, a portion of a drain region of the first transistor, and a source and drain region of the second transistor, implementing ESD implantation under the regions without the patterned mask layer, removing the mask layer and forming sidewall spacers of the gates, and implementing drain diffusion.